IRPLLED1

IRPLLED1 350mA to 1.5A High Voltage LED Driver using IRS2540

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EVALUATION BOARD - IRPLLED1

1. Introduction

As the industry becomes more power conscious to compensate for increasing energy costs and to meet governmental regulations, new innovative ways of conserving energy are being developed. For the lighting industry one of these outlets has been LEDs. Due to their longevity, robust design, low maintenance and high efficiency, they have proven a viable alternative to less efficient light sources. With their long term projected falling cost and further increased efficiency, the industry has eagerly embraced LEDs, putting them largely in demand. LEDs require drivers that have specific features such as constant current control over the temperature and manufacturing variations of LEDs, dimming and appropriate fault protections. The IRS2540/1 is specifically designed to address these requirements

The IRPLLED1evaluation board is a high voltage LED driver designed to operate from a DC input voltage of 50V to 170V and produce an output voltage of 16V-24V to supply a programmable load current of 350mA, 700mA, 1A, or 1.5A. It uses the IRS2540/1, a high voltage, high frequency Buck control IC for constant LED current regulation. The IRS2540/1 controls the average load current by a continuous mode time-delayed hysteretic method using an accurate on chip band gap voltage reference. The 8-pin, 200V/600V rated IRS2540/1 inherently provides short-circuit protection with open-circuit protection incorporated by a simple external circuit and has dimming capability. The IRS2540/1 allows scalable designs to accommodate series and parallel configurations of LEDs, for today's production LEDs as well as new generation higher current LEDs, and provides high current control accuracy over input and output voltage.

The evaluation board documentation will briefly describe the functionality of IRS2540/1, discuss the selection of the output stage, switching components and surrounding circuitry. This board was tested with a single Lumileds™ flood board for the 350mA and 700mA settings using two Lumileds flood boards in parallel to provide test loads for the 1A and 1.5A settings. Lumileds flood boards are available through Future Electronics and have a maximum nominal current rating of 700mA with a breakdown voltage between 16 and 24V. The IRPLLED1 evaluation board can operate from a 120V AC rectified line with the addition of a bridge rectifier and smoothing capacitor at the front end. It is **non-isolated** and therefore although the output voltage is low an **electric shock hazard** still exists!

2. Constant current control

The IRS2540/1 is a time-delayed hysteretic Buck controller. During normal operating conditions the output current is regulated via the IFB pin voltage to a nominal value of 500mV. This feedback signal is compared to an internal high precision band gap voltage reference. An on-board dV/dt filter has also been used to prevent erroneous transitioning. This is necessary since the IFB pin is sensitive to noise.

Once the VCC supply to the IR2540 reaches V_{CCUV+} the LO output is held high and the HO output low for a predetermined period of time. This initiates charging of the bootstrap capacitor establishing the VBS floating supply for the high side output. The chip then begins toggling HO and LO outputs as needed to regulate the load current. monitored and fed back through RCS shown in fig 1 The deadtimes of approximately 140ns between the LO and HO gate drive signals prevent "shoot through" and reduce switching losses, particularly at higher frequencies.

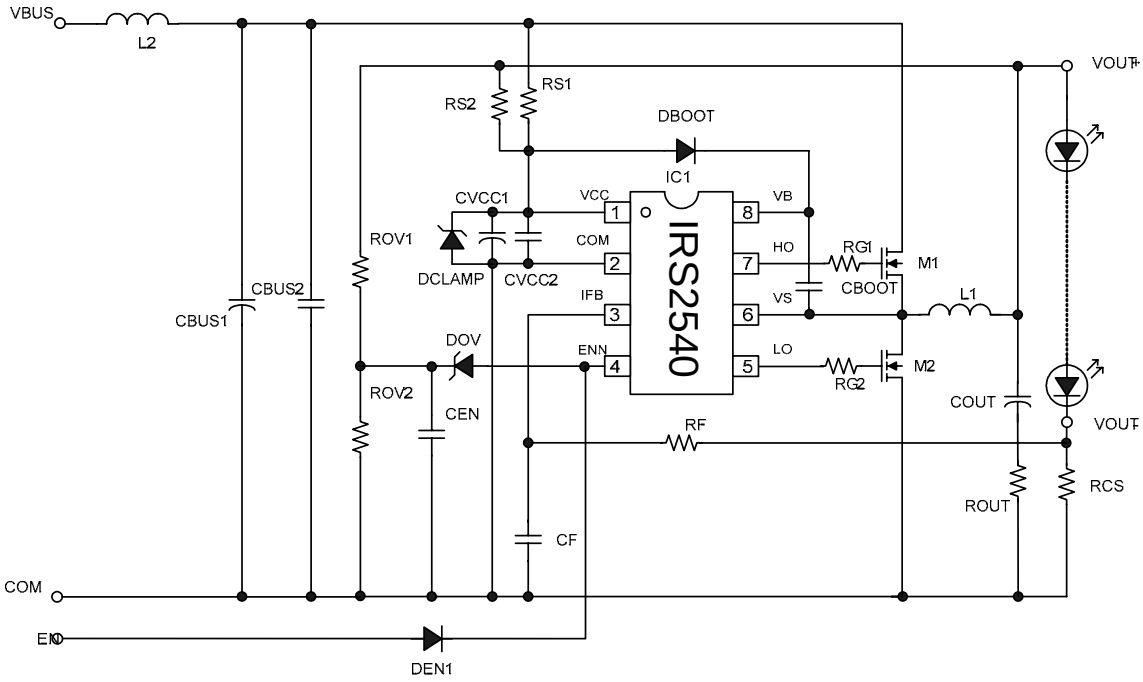
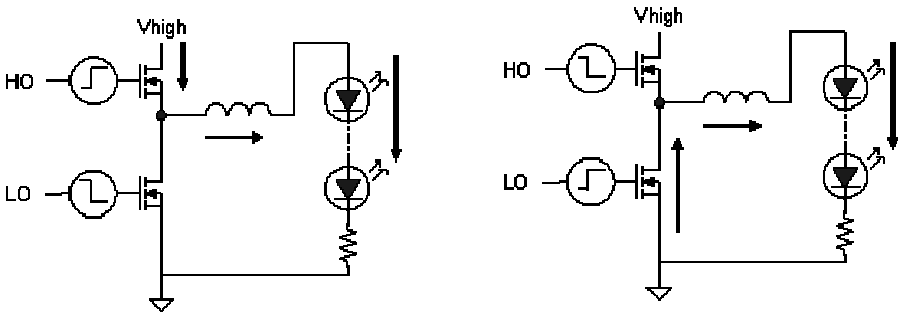


Fig. 1 IRS2540/1 Constant Current LED Driver Typical Schematic
(see Fig. 16 for evaluation board full schematic)

Note: Rout is needed only in few applications

Under normal operating conditions, if VIFB is below VIFBTH, HO is high and the load receives current from VBUS through L1. This simultaneously stores energy in the output stage comprised of L1 and COUT, whilst VIFB begins to increase. When VIFB crosses VIFBTH, HO goes low after the delay t_HO_off. Once HO is low, LO will transition high after the deadtime. The inductor and output capacitor release the stored energy into the load and VIFB starts decreasing. When VIFB crosses VIFBTH again, LO switches low after the delay t_LO_off and HO switches high after the delay t_HO_on.



(A) **(B)**

Fig. 2 (A) Storing Energy in Inductor
(B) Releasing Stored Inductor Energy

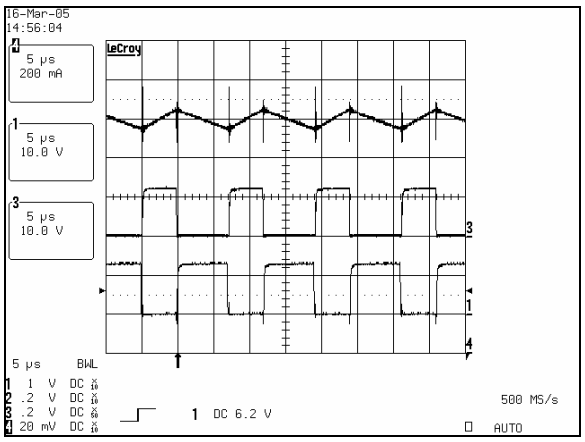


Fig. 3 IRS2540/1 Control Signals, Iavg=1.2A

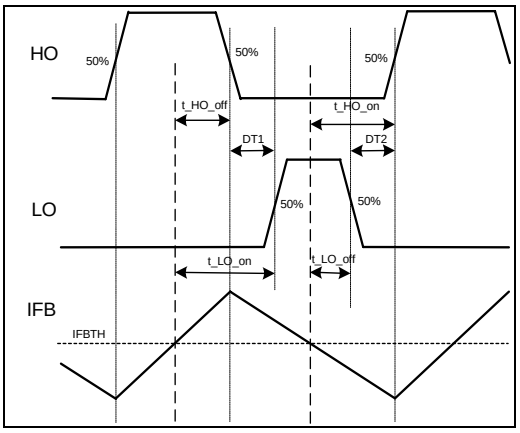


Fig. 4 IRS2540/1 Time Delayed Hysterisis

The switching continues to regulate the current at an average value determined as follows: when the output combination of L1 and COUT is large enough to maintain a low ripple on IFB (less than 100mV), Iout(avg) can be calculated:

$$Iout(avg) = {VIFBTH}/{RCS}$$

Having load current programmable from 350mA to 1.5A, series and parallel combinations of resistors must be used to correctly set the current as well as distribute power accordingly. Equivalent resistances for each current setting are calculated as follows:

$$R_{350mA} = \frac{0.5V}{350mA} = 1.43\Omega$$

$$R_{700mA} = \frac{0.5V}{700mA} = 0.71\Omega$$

$$R_{1A} = \frac{0.5V}{1A} = 0.5\Omega$$

$$R_{1.5A} = \frac{0.5V}{1.5A} = 0.33\Omega$$

Since some of these equivalent values of resistance are not available, series and parallel combinations are used and are specified as follows (all combinations use standard value resistors: 1.43Ω, 0.56Ω, and 0.47Ω):

$$R_{350mA} = 1.43\Omega$$

$$R_{700mA} = 0.71\Omega \approx (1.43\Omega \,||\, 1.43\Omega) = 0.715\Omega$$

$$R_{1A} = 0.5\Omega \approx (0.47\Omega + 0.56\Omega) \,||\, (0.47\Omega + 0.56\Omega) = 0.515\Omega$$

$$R_{1.5A} = 0.33\Omega \approx (0.47\Omega + 0.56\Omega) \,||\, (0.47\Omega + 0.56\Omega) \,||\, (0.47\Omega + 0.56\Omega) = 0.343\Omega$$

Although some of the series and parallel combinations do not yield the exact resistance needed for tolerance purposes, they are accurate enough. For this evaluation board an extremely tight current regulation is achieved with a worst case result of ±1.2% for the 350mA setting over the bus voltage range from 50V to 170V. Likewise a precise regulation of ±0.25% can be maintained for a range of load voltage from 16V to 24V at the 350mA current setting. The jumper positions on the evaluation boards (JSET) for setting the different load currents are shown below:

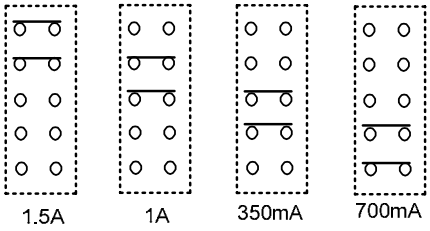


Fig. 4a: JSET LED Current Programming Settings

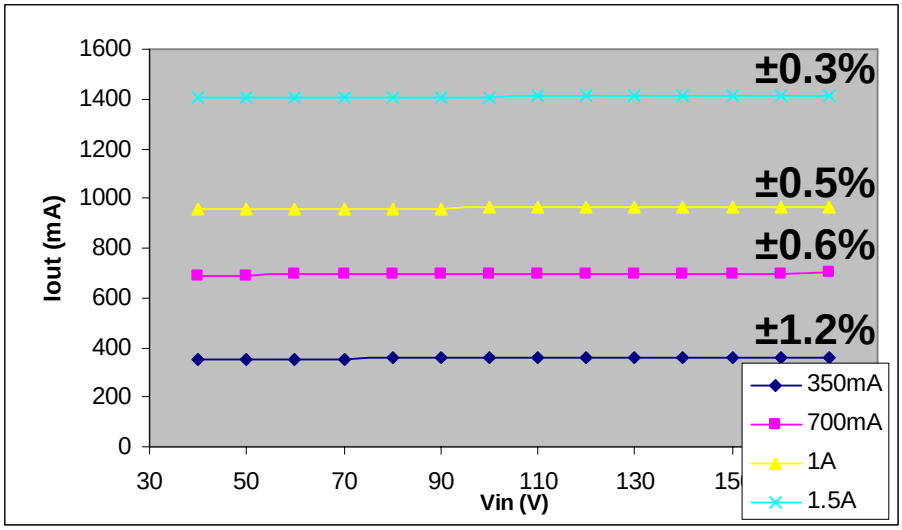


Fig. 5 Vout = 16V, L1 = 470uH, COUT = 33uF

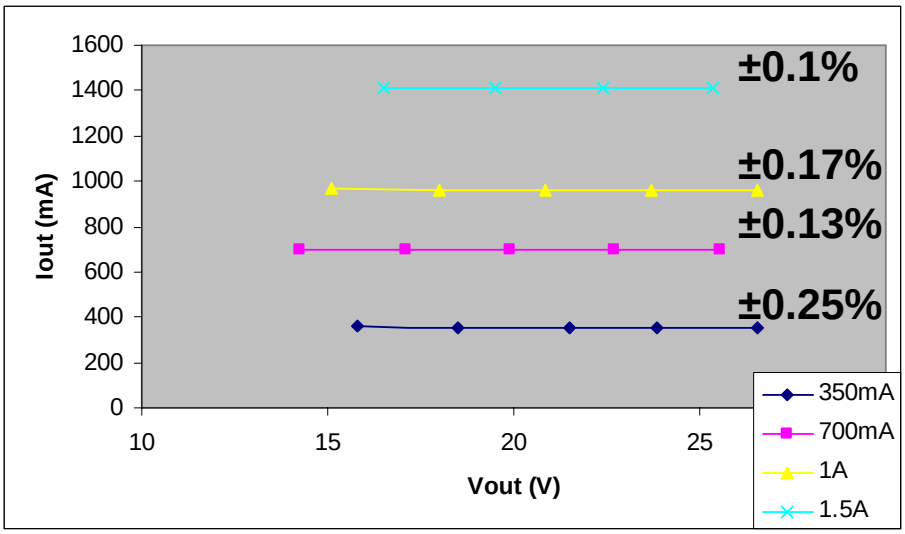


Fig. 6 Vbus = 100V, L1 = 470uH, COUT = 33uF

3. Frequency selection

The frequency in the IRS2540/1 application is free running and maintains current regulation by quickly adapting to changes in input and output voltages. There is no need for additional external components to set the frequency as seen with most oscillators. The frequency is determined by L1 and COUT, as well as the input/output voltages and load current. The selection of the frequency is a trade-off between system efficiency, current control regulation, size, and cost.

The higher the frequency, the smaller and lower the cost of L1 and COUT, the higher the ripple, the higher the FET switching losses, which becomes the driving factor as VBUS increases to higher voltages, the higher the component stresses and the harder it is to control the output current.

With an input voltage as high as 170V, the targeted frequency was determined to be between 50kHz and 75kHz. Within these operating conditions all components can withstand their associated power losses.

4. Output L1 and COUT selection

To maintain tight hysteretic current regulation L1 and COUT need to be large enough to maintain the supply to the load during t_HO_on and avoid significant undershooting of the load current, which in turn causes the average current to fall below the desired value.

First, we are going to look at the effect of the inductor when there is no output capacitor to clearly demonstrate the impact of the inductor. In this case, the load current is identical to the inductor current. Fig. 7 shows how the inductor value impacts the frequency over a range of input voltages. As can be seen, the input voltage has a great impact on the frequency and the inductor value has the greatest impact at reducing the frequency for smaller input voltages.

Fig. 8 shows how the variation in load current increases over a span of input voltage, as the inductance is decreased. Fig. 9 shows the variation of frequency over different output voltages and different inductance values. Finally Fig. 10 shows how the load current variation increases with lower inductance over a range of output voltages.

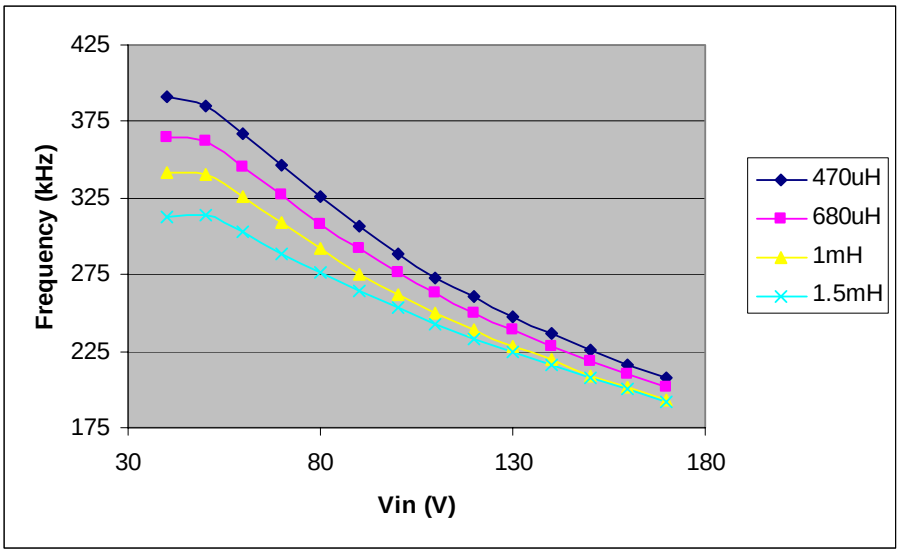


Fig. 7 Iout = 350mA, Vout = 16.8V, COUT = 0uF

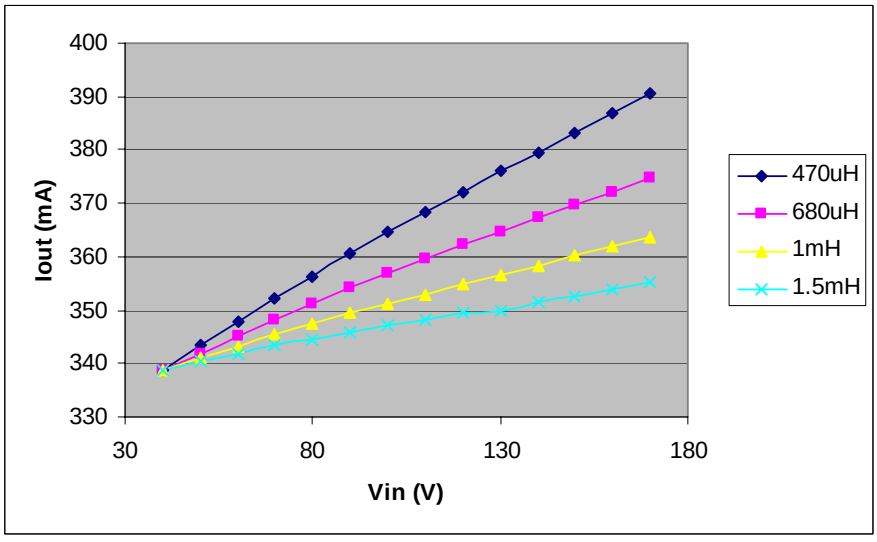


Fig. 8 Iout = 350mA, Vout = 16.8V, COUT = 0uF

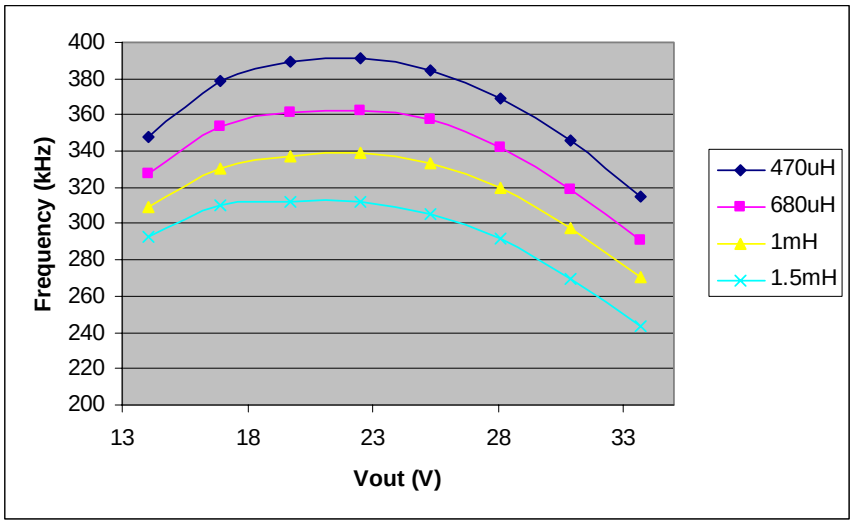


Fig. 9 Iout = 350mA, Vin = 50V, COUT = 0uF

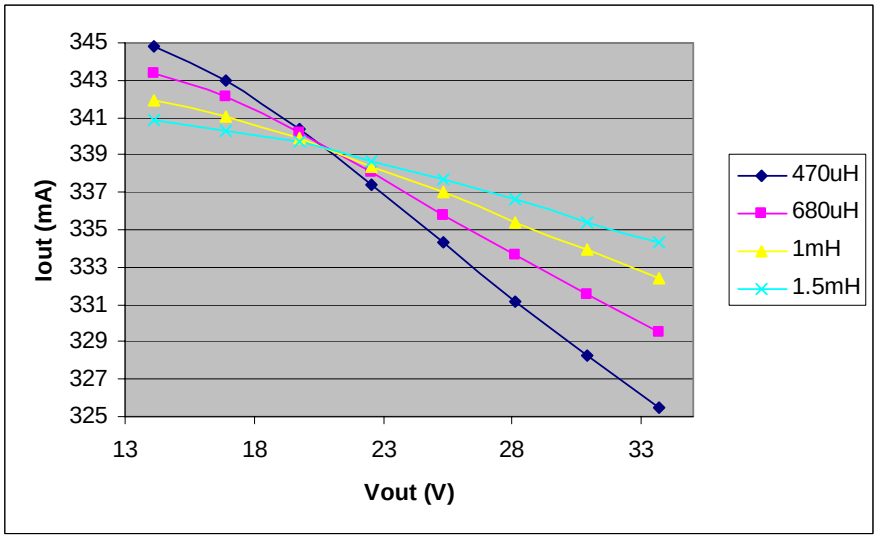


Fig. 10 Iout = 350mA, Vin = 50V, COUT = 0uF

The output capacitor can be used simultaneously to reduce the frequency and improve current control accuracy. Fig. 11 shows how the capacitance reduces the frequency over a range of input voltage. A small capacitance of 4.7uF has a large effect on reducing the frequency. Fig. 12 shows how the current regulation is also improved with the output capacitance. There is a point at which continuing to add capacitance no longer has a significant effect on the operating frequency or current regulation, as can be seen in Fig. 12 and Fig. 13.

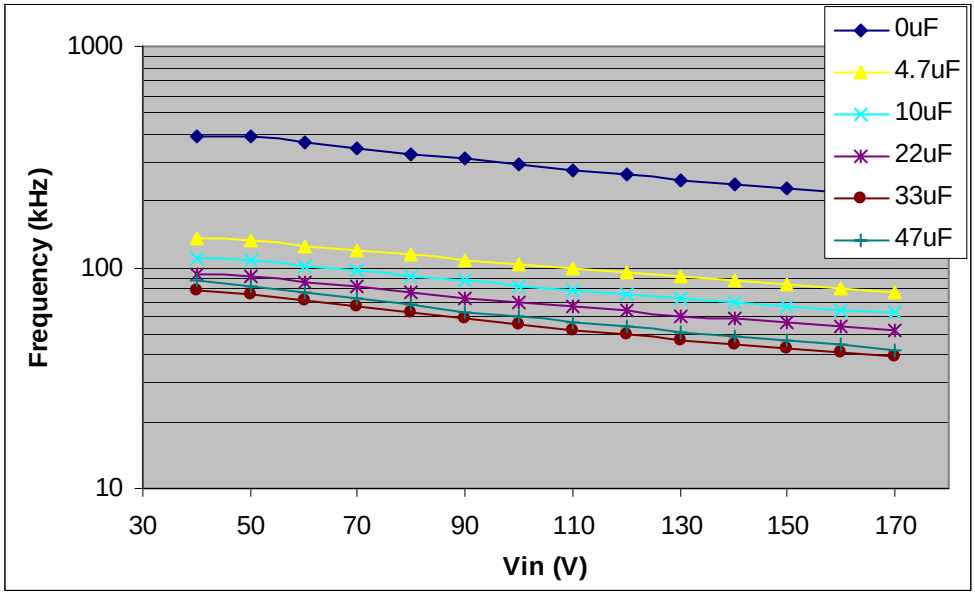


Fig. 11 Iout = 350mA, Vout = 16.8V, L = 470uH

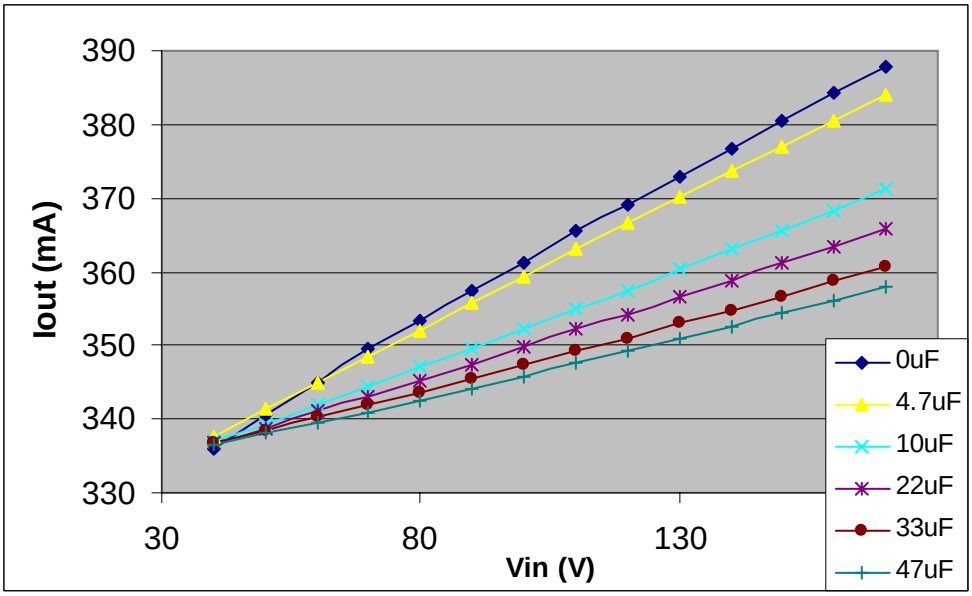


Fig. 12 Iout = 350mA, Vout = 16.8V, L = 470uH

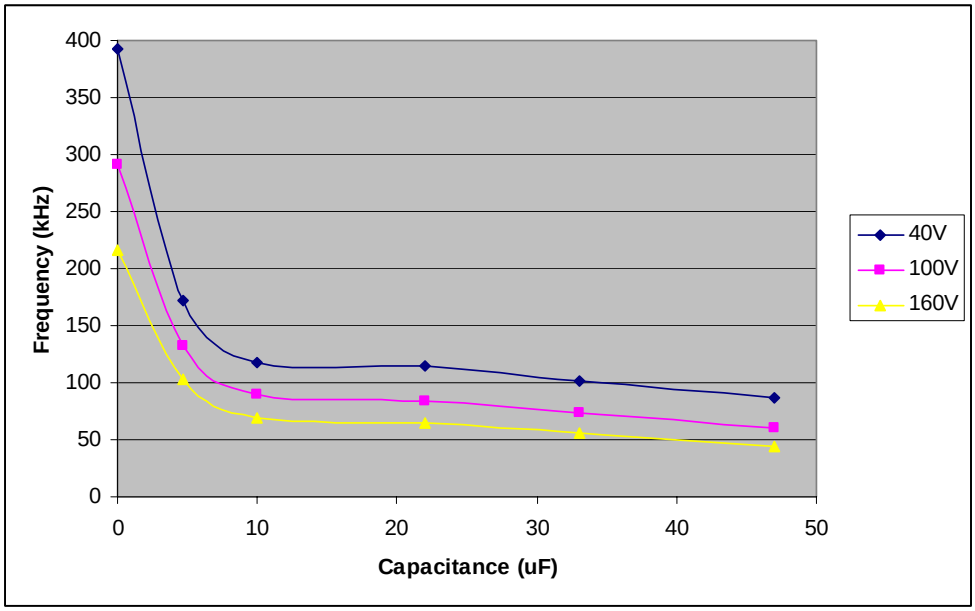


Fig. 13 Iout = 350mA, Vout = 16.8V, L = 470uH

The addition of the COUT is essentially increasing the amount of energy that can be stored in the output stage, which also means it can supply current for an increased period of time. Therefore by slowing down the di/dt transients in the load, the frequency is effectively decreased.

With the COUT capacitor added to the circuit the inductor current is no longer identical to that seen in the load. The inductor current has a triangular shape, where as the load will see the same basic trend in the current, but all sharp corners become rounded with peaks significantly reduced, as can be seen in Fig. 14 and 13.

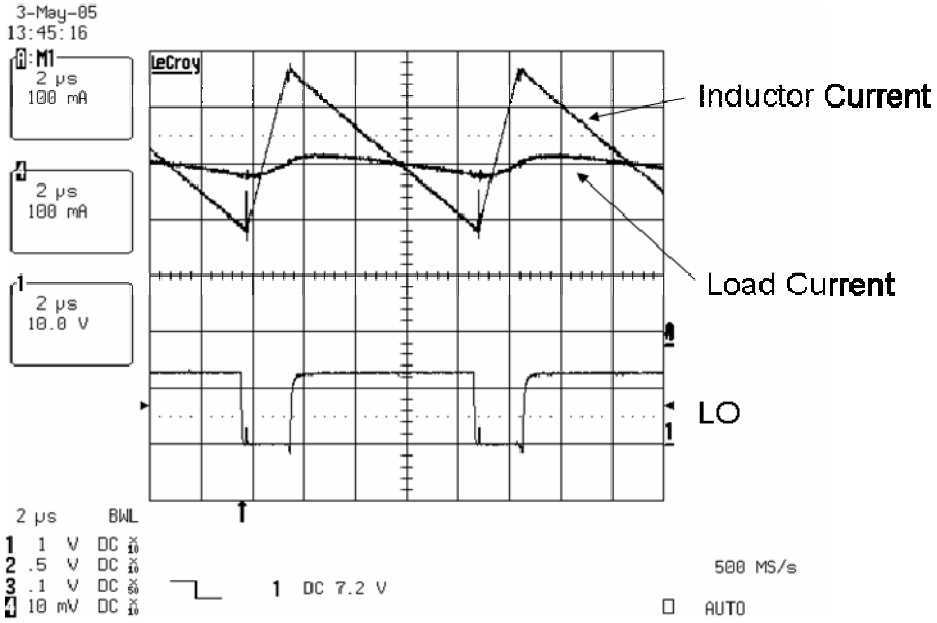


Fig. 14 Iout = 350mA, Vin = 100V, Vout = 16.85V, L = 470uH, COUT = 33uF

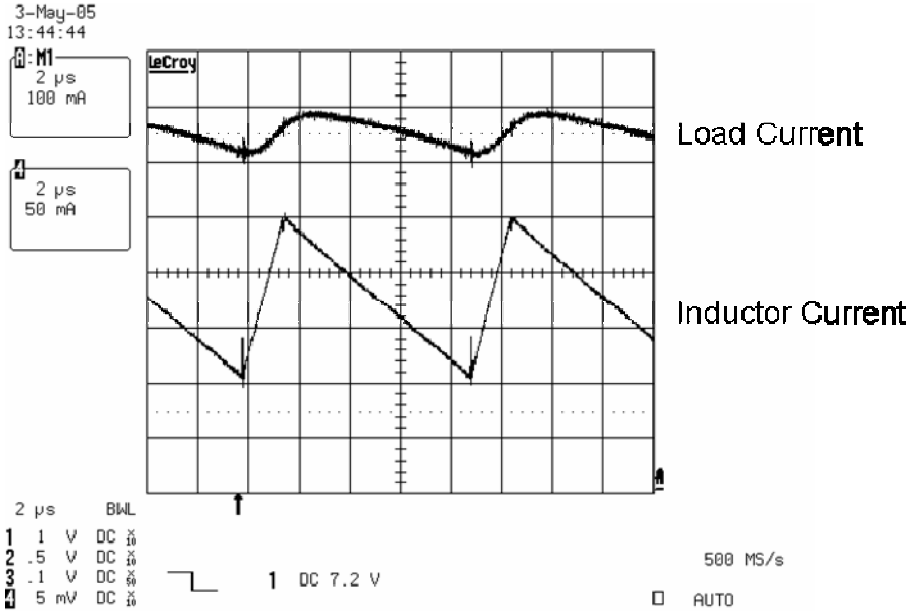


Fig. 15 Iout = 350mA, Vin = 100V, Vout = 16.85V, L = 470uH, COUT = 33uF

L1 and COUT need to be chosen so that enough energy is stored to supply the load during t_HO_on while maintaining current control accuracy. A lower value of L1 requires a larger value of COUT.

Since this evaluation board is designed to handle a load current no higher then 1.5A, off the shelf inductors are available. To minimize or eliminate any effects of eddy currents, a custom inductor for this application was designed by VOGT. Values in the order of 1mH or more of inductor that can handle this amount of current are not readily available and tend to be bulky and costly. With too small an inductor (of 100uH or less) the COUT capacitor would need to be in the order of hundreds of micro Farads to maintain good current regulation. Additionally with a smaller inductance, the ripple current seen by the capacitor would be quite large, which would shorten the life of the capacitor if an electrolytic were used.

Because of these considerations an inductor of 470uH and an output capacitance of 33uF were chosen to accommodate the 1.5A load current. The current ripple associated with 470uH is relatively small so the board can be operated with or without output capacitance at the lower current ratings.

5. MOSFET vs Diode for the low side switch

The IRS2540/1 has been designed so that it can drive a low side MOSFET and a high side MOSFET. Alternatively the low side FET can be replaced by a freewheeling diode as shown in Fig. 16. This may yield a lower cost system, but there are some efficiency tradeoffs to be considered, particularly for higher load currents. The system efficiency is directly influenced by several system parameters including operating frequency, load current, and input voltage. In this evaluation board a fast recovery power diode is used for the lower switch.

A major parameter to consider is the reverse recovery time of the diode in comparison to the body diode of the FET it replaces. The diode intrinsically has a much shorter reverse recovery time since the device is specifically designed for this, where as the body diode is a parasitic element that originates from basic processing technology and typically has inferior characteristics, in terms of forward drop, reverse recovery, and power handling capabilities.

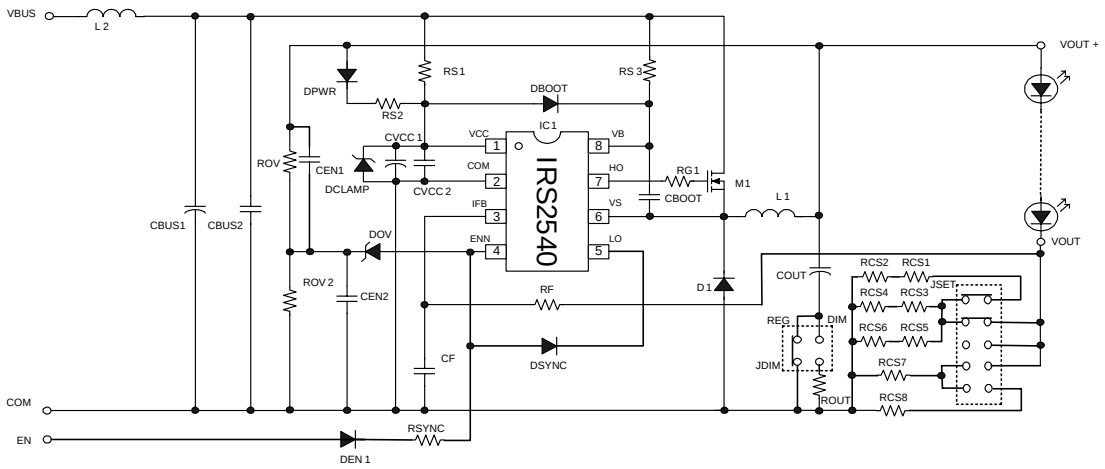


Fig. 16 Alternate IRS2540/1 Time-Delayed Hysteretic Controlled Evaluation Board Schematic

Note: Rout is needed only in few applications

The reverse recovery problem is incurred during the deadtime after the low side MOSFET has been on and conducting current. During this deadtime the lowside MOSFET is off, but the body diode is freewheeling and providing current to the load. Since the body diode is conducting current, carriers are present and will eventually need to be recombined, leading to reverse recovery delay. When the high side MOSFET turns on the VS node is very rapidly pulled from COM to VBUS and the low side MOSFET or the freewheeling diode conducts current from VS to ground due to the reverse recovery effect, potentially resulting in large power losses. This can result in overheating of the low side switching component and component stress, as can be seen in Fig. 17 to 18. Since the power diode has a much shorter reverse recovery time the diode will conduct current for a significantly shorter period and exhibit lower power losses. At lower frequency and reduced load current, the long recovery time associated with the MOSFET body diode may not be an issue. For higher frequency higher current applications a diode could provide lower power losses with respect to a MOSFET.

In this evaluation board the reverse recovery current peaks using a low side MOSFET could be on the order of 8A, which puts a lot of stress on the components and creates increased operating temperature. By replacing the low side MOSFET with an appropriate freewheeling diode the reverse recovery current peaks are reduced and limited to 4.5A. The frequency was also selected to keep the diode reverse recovery associated power losses low.

With the inclusion of a freewheeling diode instead of a lowside MOSFET comes the need for RS3 and DVCC. Without an initial pulse to come from LO to switch on the lower MOSFET and establish a ground reference for CBOOT to charge, an alternative means of charging CBOOT must be established. RS3 allows this charging path to exist without any interference from the chip Vcc, likewise DVCC also allows this path to remain isolated. As the bus voltage is increased, the path will allow CBOOT to fully charge and remain charged until the chip comes out of UVLO. At which time the self powering feature will take over after the first pulse from HO and the ground reference will then be created by the freewheeling diode.

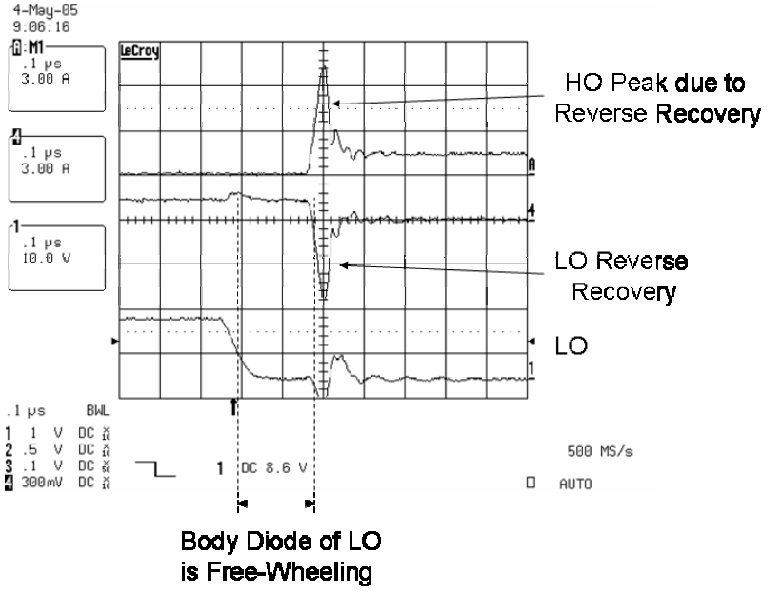


Fig. 17 Using a low side FET, Vin = 100V, Iout = 1.5A, Vout = 17V

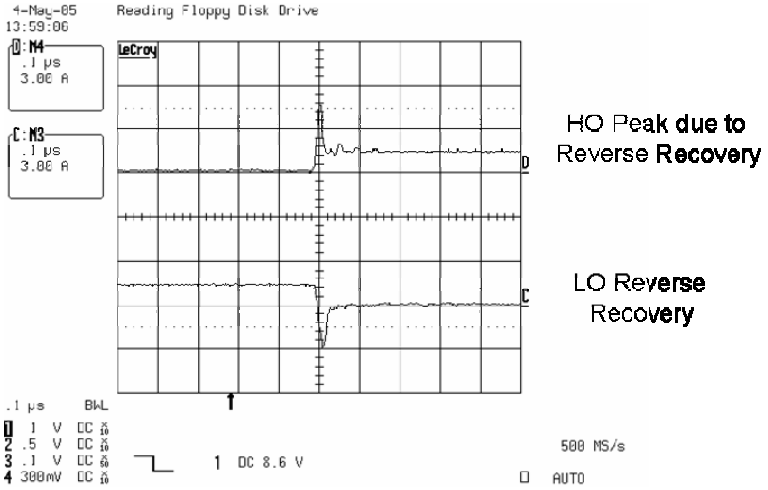


Fig. 18 Using a diode on the low side, Vin = 100V, Iout = 1.5A, Vout = 17V

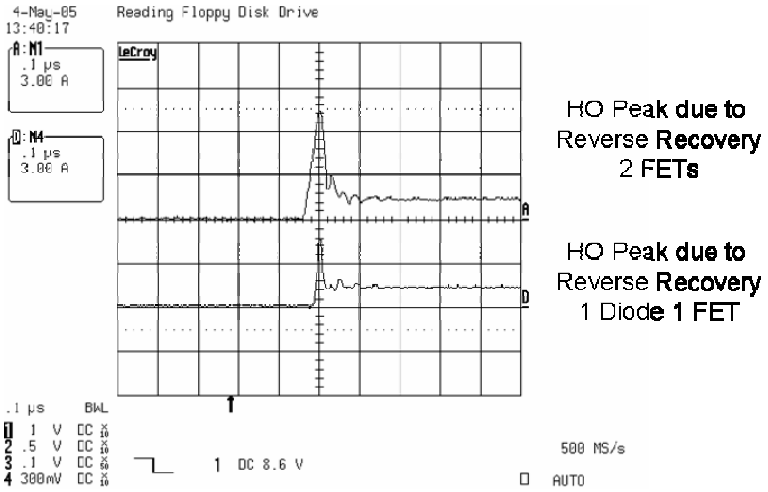


Fig. 19 Low side FET vs. low side diode comparison, Vin = 100V, Iout = 1.5A, Vout = 17V

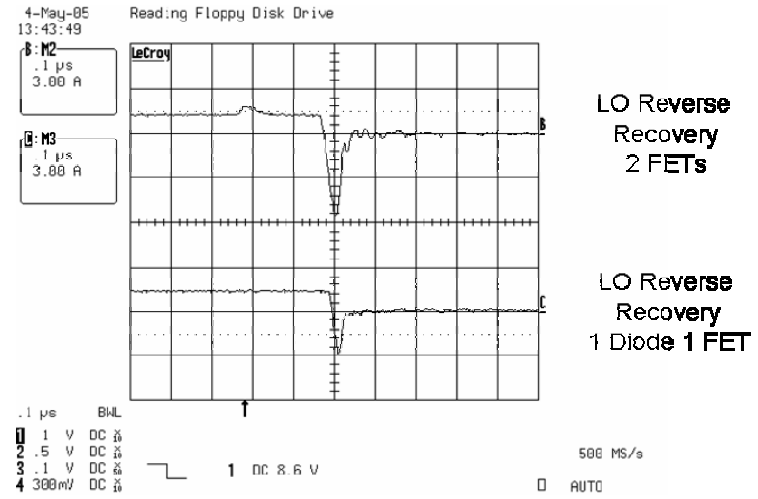


Fig. 20 Low side FET and low side diode comparison, Vin = 100V, Iout = 1.5A, Vout = 17V

The bus voltage is also of importance since it will determine how long the lowside MOSFET or the freewheeling diode will be conducting. If the bus voltage is very large in comparison to the output, the lowside MOSFET or diode will conduct for the majority of the switching period. A MOSFET has much lower on-state losses due to the low RDSon where as high voltage diodes have forward drops of approximately 1V. If the load current is in the order of 1A or 1.5A a MOSFET may have low on-state losses, where as a diode may experience larger conduction losses. If the load current is only a few hundred milliamps the losses observed in the diode may not be a concern. For system efficiency the forward conduction losses of a diode can also be compared to the reverse recovery losses with a low side MOSFET. For this evaluation board, it was found that conduction losses were less than reverse recovery losses when running at 1.5A and therefore uses and freewheeling diode.

The most efficient solution would be to put the MOSFET in parallel with the diode in the lowside position. In this case, during the deadtime, instead of the body diode freewheeling the additional diode would be conducting. This will always be the case as long as the forward drop of the external diode is less than that of the body diode.

A detailed evaluation of system needs and cost should be performed prior to choosing a MOSFET or diode for the low side. Although a diode is cheaper, in certain cases the associated power losses may require a heatsink, nullifying the cost reduction of using a diode. Likewise there are conditions where a MOSFET may prove less efficient, in which case more money will be spent on the MOSFET as well as the heatsink if required. The evaluation board is provided with a freewheeling diode and the footprint for a low side MOSFET has been provided to replace the diode with a MOSFET if required. It is not recommended to replace the diode with a MOSFET for the 1A and 1.5A operation because of the associated reverse recovery power losses.

In terms of selecting the correct MOSFET, it is best to use a part with RDSon low as possible. MOSFET parameters degrade as the voltage ratings go up. Therefore, if a 600V MOSFET is used in a 200V application, extra losses may be incurred due to a component that far exceeds the requirements. If using two MOSFETs the next parameter to be considered is the reverse recovery time. Obviously MOSFETs will not have a reverse recovery time comparable to diodes but a reverse recovery time in the order of 150 to 200ns is possible. The two remaining parameters to consider are direct trade-offs of each other, on resistance and gate charge. If the MOSFET has a relatively low gate capacitance, the die size will be small, which will result in a larger on resistance that could potentially be a problem for high current applications. On the other hand, if the MOSFET has a larger gate capacitance, the die will be relatively large and the part will have a lower on resistance. In this case more current is needed to turn on the MOSFET therefore requiring more VCC current in the IRS2540 and resulting in hgigher losses. There has to be a direct compromise between the two. Typically the best solution is a MOSFET with a relatively low RDSon and a medium sized gate capacitance, much like the device chosen for this application

6. VCC Supply

Since the IRS2450/1 is rated for 200V/600V VBUS can rvary considerably in different applications. If a simple supply resistor from VBUS is used for VCC it will experience high power losses at higher bus voltages. For higher voltage applications therefore an alternate V_{CC} supply scheme utilizing a resistor feed-back (RS2) from the output needs to be implemented, as seen in Fig. 1 and Fig. 16. This solution is limited to applications where the LED string voltage exceeds the voltage required to drive VCC, which is about 13V to guarantee good operation.

The resistance between VBUS and V_{CC} (RS1) should be large enough to minimize the current sourced directly from the input voltage line. Through this supply resistor a current will flow to charge the V_{CC} capacitor. Once the capacitor is charged up to the V_{CCUV+} threshold, the IRS2540/1 begins to operate activating the LO and HO outputs. After the first few cycles of switching the resistor RS2 connected between the output and V_{CC} will take over and source current for VCC from the output. The RS2 resistor provided in the evaluation board has been designed for an output of roughly 20V. If a higher output voltage is desired, RS2 will need to be redesigned and adjusted accordingly. Conversely, if the output voltage is below 20V the value of RS2 may need to be reduced in order to supply sufficient voltage to VCC.

A 10uF capacitor has been used at VCC of the IRS2540, which removes most low frequency ripple that could originate from VBUS due to a rectified voltage waveform.

If the input and output voltages are defined for the evaluation board, enough information is provided to calculate values for RS1, RS2, and RS3 (see Fig. 23 for component definition). All three supply resistors were chosen to be 1W devices since they source all current to the chip. Efficiency can be improved by optimizing these values for specific applications.
By making each component 1W, the work in supplying VCC can be split up equally making it a more robust solution instead of relying entirely on one component. This also allows the chip to turn on at a lower bus voltage.

Assuming that a 14V external zener diode will be used on Vcc, exact values of RS1, RS2, and RS3 are calculated as follows (values calculated to operate the components just below half their rated power):

$$P = V^2 / R$$

RS1

$$\tfrac{1}{2}W = \frac{\left(V_{Bus_{\max}} - 14V\right)^2}{RS1}$$

$$RS1 = \frac{\left(V_{Bus_{\max}} - 14V\right)^2}{\tfrac{1}{2}W} = \frac{\left(170V - 14V\right)^2}{\tfrac{1}{2}W}$$

$$RS1 = 48.6k\Omega \approx 56k\Omega$$

RS3

min duty ratio ≈ 10%

$$\tfrac{1}{2}W = \frac{(1-0.1)\cdot\left(V_{Bus_{\max}} - 14V\right)^2}{RS3}$$

$$RS3 = \frac{(1-0.1)\cdot\left(V_{Bus_{\max}} - 14V\right)^2}{\tfrac{1}{2}W} = \frac{(1-0.1)\cdot\left(170V - 14V\right)^2}{\tfrac{1}{2}W}$$

$$RS1 = 43.8k\Omega \approx 47k\Omega$$

RS2

$$\tfrac{1}{2}W = \frac{\left(V_{Out_{\max}} - 14V\right)^2}{RS2}$$

$$RS2 = \frac{\left(V_{Out_{\max}} - 14V\right)^2}{\tfrac{1}{2}W} = \frac{\left(30V - 14V\right)^2}{\tfrac{1}{2}W}$$

$$RS1 = 512\Omega \le 1k\Omega$$

RS1 may be rounded up to 1K

7. VBS Supply

The bootstrap diode (DBOOT) and supply capacitor (CBOOT) comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before operation commences, the first pulse from the output drivers comes from the LO pin. During under voltage lock-out mode, the high and low-side outputs are both held low.

During an open circuit condition, without the watchdog timer, the HO output would remain high at all times and the charge stored in the bootstrap capacitor (CBOOT) would slowly leak until reaching zero, thus eliminating the floating power supply for the high side driver. To maintain sufficient charge on CBOOT, a watchdog timer has been implemented. In the condition where VIFB remains below VIFBTH, the HO output will be forced low roughly after 20µs and the LO output forced high. This toggling of the outputs will last for 1µs to maintain and replenish sufficient charge on CBOOT.

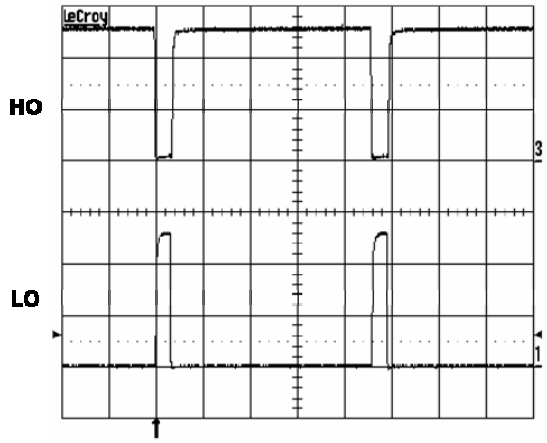


Fig. 21 Illustration of Watchdog Timer

The bootstrap capacitor value needs to be chosen so that it maintains sufficient charge for at least the 20µs interval until the watchdog timer allows the capacitor to recharge. If the capacitor value is too small, the charge will fully dissipate in less than 20µs. The bootstrap capacitor should be at least 100nF. A larger value within reason can be used if preferred.

The bootstrap diode should be a fast recovery, if not an ultrafast recovery component to maintain good efficiency. Since the cathode of the bootstrap diode will be switching between COM and VBUS + 14V, the reverse recovery time of this diode is of critical importance. For additional information concerning the bootstrap components, refer to the Design Tip (DT 98-2), *"Bootstrap Component Selection For Control ICs"* at www.irf.com under Design Support.

8. Enable Pin

The enable pin can be used for dimming or open-circuit protection. When the ENN pin is held low the IRS2540 remains in a fully functional state with no alterations to the operating environment. To disable the control feedback and regulation a voltage greater than VENTH (approximately 2.5V) needs to be applied to the ENN pin. With the chip in a disabled state the HO output will remain low and the LO output will remain high to prevent VS from floating, in addition to maintaining charge on the bootstrap capacitor if a MOSFET is used for the lower switch. The threshold for disabling the IRS2540/1 has been set to 2.5V to enhance immunity to any externally generated noise or application ground noise and also makes it possible receive a drive signal from a microcontroller.

Dimming Mode

To achieve dimming a signal with constant frequency and set duty cycle can be fed into the ENN pin. There is a direct linear relationship between the average load current and duty cycle if no output capacitor is used in the circuit. A large output capacitor tends to increase the minium dim level because some current continues to supply the LEDs from this capacitor during the off phase of the PWM dimming. With no output capacitor, if the ratio is 50% then 50% of the maximum set light output will be emitted. Similarly if the ratio is 30% then 70% of the maximum set light output will be realized. A sufficiently high frequency of the dimming signal must be chosen to avoid visible

flashing or “strobe light” effect. A signal around 1kHz from zero to 5V is recommended. For this evaluation board, a fully adjustable (0% to 100% duty cycle) PWM wave generator is suggested but this is not included as part of the evaluation board. The following circuit is a simple enable pin dimming signal generator.

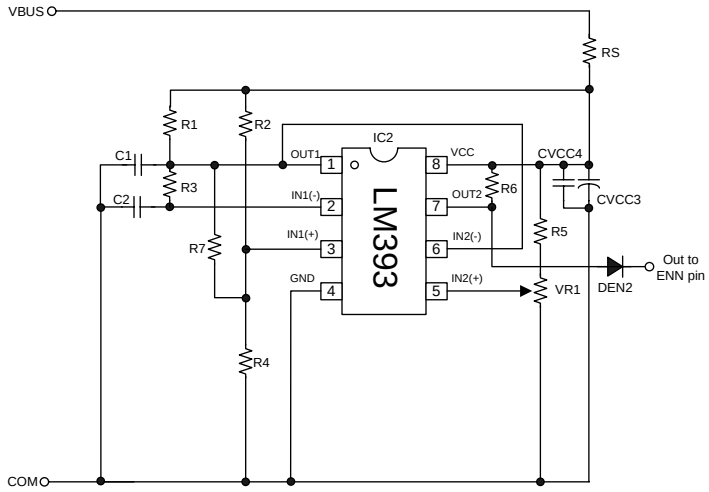


Fig. 22 Suggested PWM Driver (not included in IRPLLED1.5X2)

If an external supply for VCC is used, the minimum amount of dimming achievable (light output approaches 0%) will be determined by the “on” time of the HO output, when in a fully functional regulating state. To maintain reliable dimming, it is recommended to keep the “off” time of the enable signal at least 10 times that of the HO “on” time. For example, if the application is running at 75kHz with an input voltage of 100V and an output voltage of 20V, the HO “on” time will be 2.7µs (one-fourth of the period – see calculations below) according to standard buck topology theory. This will set the minimum “off” time of the enable signal to 27µs.

$$Duty\ Cycle = \frac{V_{out}}{V_{in}} * 100 = \frac{20V}{100V} * 100 = 20\%$$

$$HO_{on\ \mathrm{time}} = 20\% * {}^{1}\!\diagup\!_{75kHz} = 2.7\mu s$$

If the IRS2540 is supplied from the output, a large enough capacitor on VCC is required to maintain sufficient current while in a disabled state. For this evaluation board where the IC supply comes from the output, a 10uF capacitor is used to ensure continued operation while disabled. The output is capable of dropping to roughly 10V. A “strobe light” effect in the LEDs may be observed if VCC drops too much or if the dimming frequency is too low.

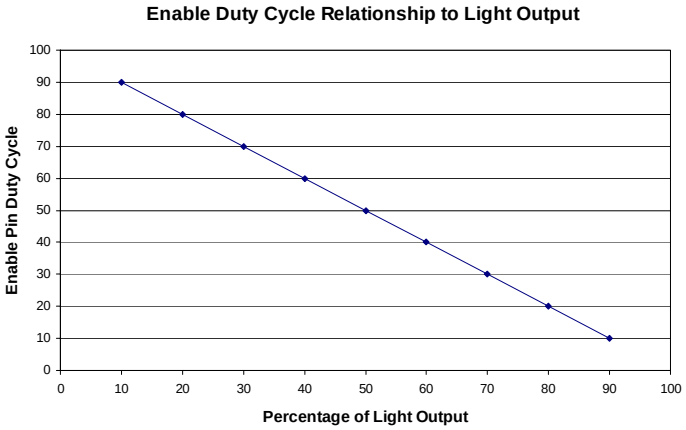


Fig. 23 Light Output vs Enable Pin Duty Cycle

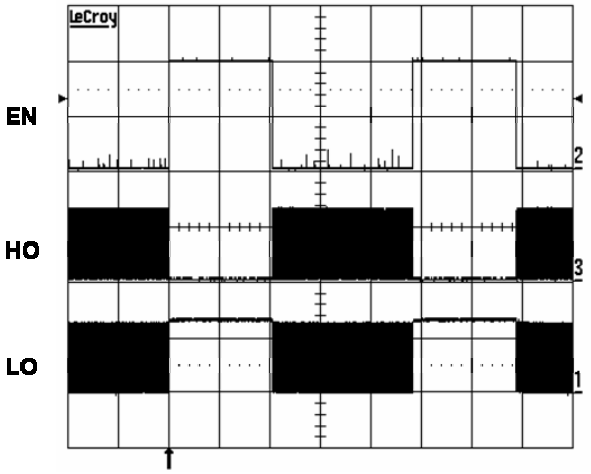


Fig. 24 IRS2540 Dimming Signals

Since the IRS2540/1 does not include an onboard oscillator, a soft start feature is not easily implemented. This is only a concern when operating in the dimming mode. Since PWM dimming is required of LEDs, the output is essentially turning on and off at a rate of the dimming frequency. In the absence of soft start a large spike of current would be observed in the load each time the output is turned on. This current spike stresses the load possibly decreasing LED operating lifetime. The IRPLLED1includes a jumper setting to define whether or not the board is being used in the dimming mode. This two position jumper allows the designer to either include or exclude the resistor Rout, which is in series with the output capacitor. The inclusion of this resistor will sufficiently damp the output stage, such that output current spikes are reduced or eliminated. The presence of such current spikes may cause the inductor to hum or buzz where the emitted sound will be that of the dimming frequency. The inrush of current causes mechanical movement in the inductor which can be heard since the PWM signal is within the audible range of the human ear. The effects of adding in Rout can be seen in Fig. 25 – 28.

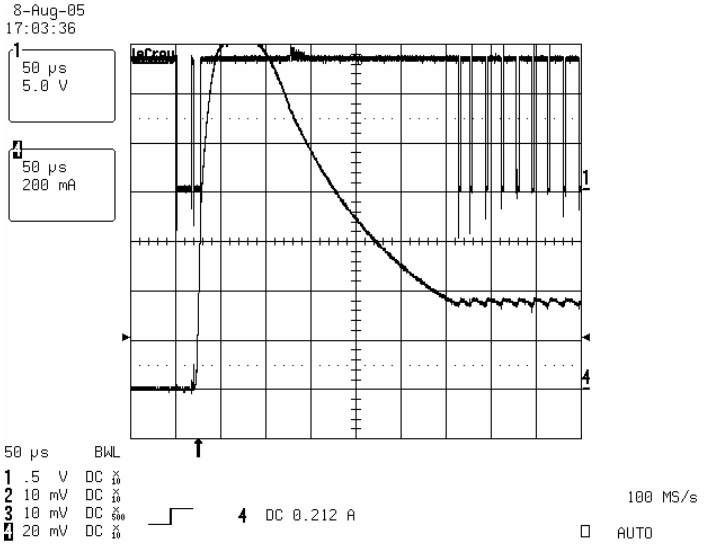


Fig. 25 Load Current Spike Excluding Rout
Iout = 350mA, Vin = 100V, Vout = 17V

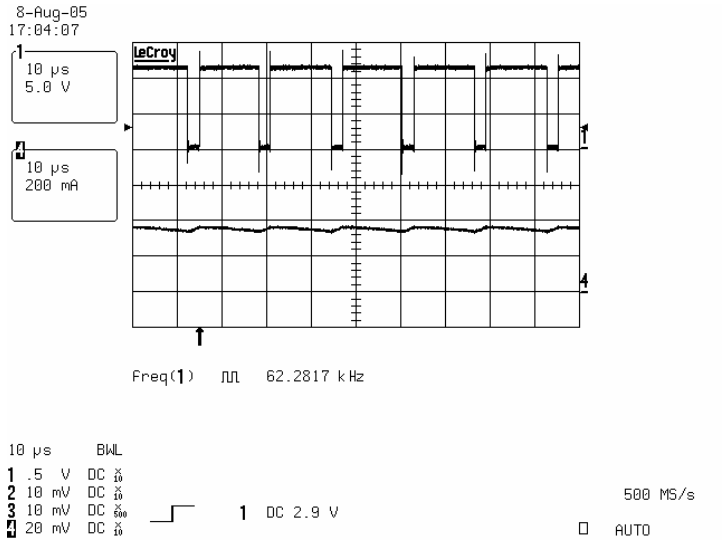


Fig. 26 Load Current Ripple Excluding Rout
Iout = 350mA, Vin = 100V, Vout = 17V

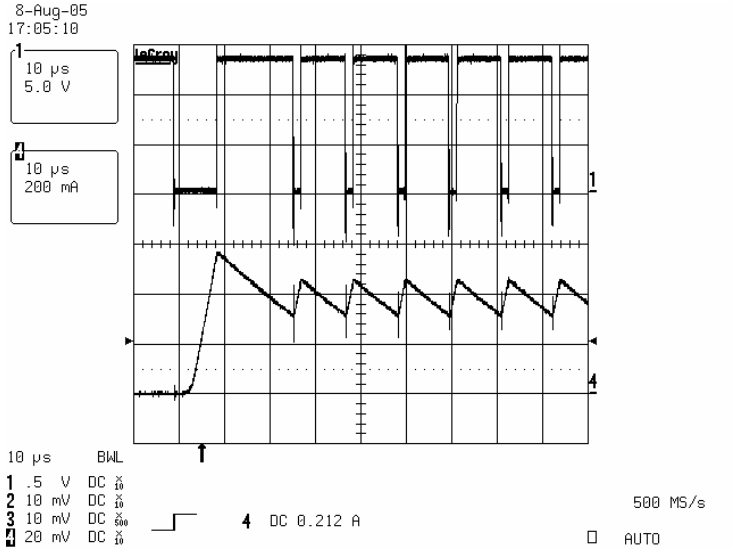


Fig. 27 Load Current Spike Including Rout (5ohm)
Iout = 350mA, Vin = 100V, Vout = 17V

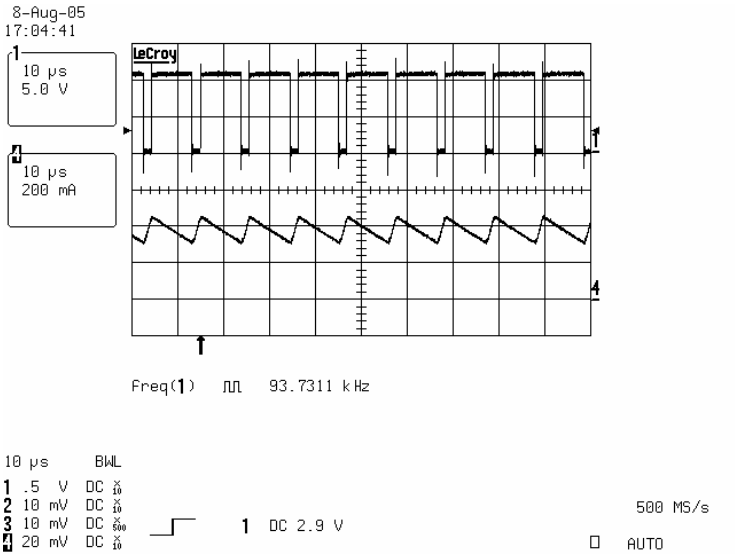


Fig. 28 Load Current Ripple Including Rout (5ohm)
Iout = 350mA, Vin = 100V, Vout = 17V

Although the inclusion of the resistor Rout minimizes or eliminates the load current spikes, the overall current regulation and operating frequency will be slightly compromised. The resistor reduces the overall effectiveness of the output capacitor, which means the switching frequency will marginally increase. The output ripple current will also increase, which ultimately leads to a larger current regulation tolerance. Although the overall current regulation capabilities may decrease with the inclusion of this resistor, the actual stability of the PWM dimming signal will still be the dominant factor of the overall output current regulation capabilities.
It should be noted that the IRPLLED1 reference design board reflects the schematic of Figure 16 where a high speed diode is used in place of the lower MOSFET switch indicated in Figure 1.
The addition of resistor RSYNC and diode DSYNC synchronizes the ENN input signal such that, when ENN transitions from low to high to disable the oscillator during a period when HO is high, the IRS2540 will not react

until the end of the current HO cycle as shown in the waveform diagram below. The reason for this is to avoid the possibility off ENN transitioning from low to high at the exact time that HO transitions from low to high, which may trigger the HO output to latch up under a low VBS supply condition. This is caused by propagation delays that exist inside the IC. RSYNC and DSYNC are not necessary in non-dimming applications. Synchronization as described will not affect the operation or dimming functionality of the circuit. It will serve only to protect the circuit against a possible fault condition, without any detrimental effect to operation.

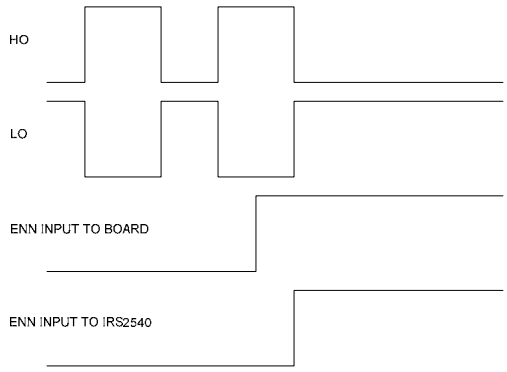


Fig. 28a: Dimming Syncronization Waveforms.

9. Open circuit protection

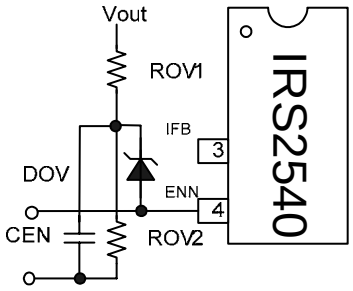


Fig. 29 Open Circuit Protection Scheme

By using the suggested voltage divider, capacitor, and zener diode, the designer can virtually clamp the output voltage at any desired value. If there is no load to clamp the output voltage, the positive output terminal will rise to the input bus voltage.

The above circuit is able to limit the output voltage in this situation. However it should be noted reducing the output voltage **does not prevent the possibility of electric shock in non-isolated systems!** Therefore an IRS2540 based Buck LED driver running directly off line would still be an electric shock hazard and it would **not** be safe to attempt to replace the LEDs if such a system were powered. In non-isolated systems, additional mechanical protection is required to ensure that access to the LEDs is not possible or alternative a mechanical isolation system could be used to disconnect the LEDs completely from the ballast for safe access. In an illuminated sign for example, this would be a reasonable approach.

The open circuit protection system described in this section can only be an effective safety feature in a system where the IRS2540 Buck stage is used as a back end stage supplied by an already isolated DC source. This scheme also conflicts with the synchronization operation described in the previous section, therefore this over-voltage protection scheme is less effective in dimming systems where the RSYNC and DSYNC modification has been added.

The open load protection circuit in Fig 29 is recommended for isolated non-dimming applications where the load may be disconnected and then reconnected without shutting down the driver. When the load is reconnected with power on this would reduce the initial surge of current to the output reducing stress on the LEDs .
Connecting the over voltage protection network to the IFB pin instead of the ENN pin in dimming systems is possible, however since this can introduce noise into the sensitive IFB pin, this is not recommended.
In an open circuit condition, switching will continue at the HO and LO outputs, whether due to the output voltage clamp or to the watchdog timer. In this state using the protection circuit of Fig 29, rather than regulating the current with the feedback pin the output voltage will be loosely regulated via the enable pin. Transients and switching will be observed at the positive output terminal as seen in Fig. 30. The difference in signal shape, between the output voltage and the IFB, is due to the capacitor CEN used to form the voltage clamp. The repetition of the spikes can be reduced by simply increasing the cap size. If VBUS is significantly larger than the desired output voltage clamp, the output voltage will become a function of VBUS. This is because of the intrinsic delays of the chip (t_LO_on, t_LO_off, t_HO_on, and t_HO_off) along with the minimum HO on time. If the load is removed, the output will clamp at the desired voltage. Then if the bus voltage is increased there could be a proportional change in the clamped voltage.

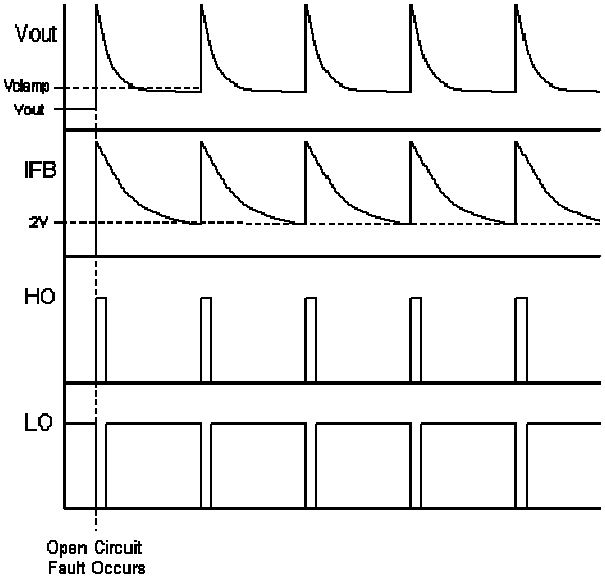


Fig. 30 Open Circuit Fault Signals, with Clamp

The two resistors ROV1 and ROV2 form a voltage divider for the output, which is then fed into the cathode of the zener diode DOV. The diode will only conduct, flooding the enable pin, when its nominal voltage is exceeded. The chip will enter a disabled state once the divider network produces a voltage at least 2.5V greater than the zener rating. The capacitor CEN serves only to filter and slow the transients/switching at the positive output terminal. The clamped output voltage can be determined by the following analysis.

$$V_{out} = \frac{(2.5V + DZ)(R_1 + R_2)}{R_2}$$

$$DZ = \text{Zener Diode Nominal Rated Voltage}$$

DOV has been chosen to be a 7.5V zener diode. ROV2 has also been set to 390Ω to help provide a low resistive charging path for CBOOT as previously discussed. It was also decided to clamp the output voltage at 30V, this is sufficiently larger than the predefined maximum load voltage of 24V as to not cause any erroneous shut-down, while it is also well within the specifications of the 100V rated output stage. Having arbitrarily chosen these parameters, ROV1 was calculated as follows:

$$V_{out} = \frac{(2.5V + DZ)(R_{OV1} + R_{OV2})}{R_{OV2}}$$

$$R_{OV1} = \frac{V_{out} R_{OV2}}{(2.5V + DZ)} - R_{OV2} = \frac{30V \cdot 390\Omega}{(2.5V + 7.5V)} - 390\Omega = 780\Omega$$

$$R_{OV1} \approx 820\Omega$$

10. Other Design Considerations

Filtering

The RC filter at the IFB pin is used to remove high frequency transients associated with the switching. The corner frequency of this filter was left high enough to prevent any further distortion of the feedback signal.

The input filter is a low-pass filter. Its main objective is to prevent ringing of comparable frequency on Vbus. Exact values of capacitance and inductance are not of critical importance, so long as adequate filtering is accomplished. In addition to the electrolytic capacitor that is used for filtering on the bus there is also a small ceramic for decoupling of high frequency noise. Ceramic capacitors typically have low ESR such that they are more ideal for high frequency filtering.

The ENN filter capacitor was arbitrarily chosen to be 100nF, this helps slow the rate of switching during open load conditions.

The IRS2540/1 was specifically designed to handle low frequency ripples on VBUS. Its capability to handle such ripple makes it ideal for an offline rectified waveform. However if high voltage (on the order of 5V-10V) high frequency oscillations (greater than or close to the operating frequency) are present on VBUS, it is recommended to implement an input filter. If these high frequency signals are present on VBUS the IRS2540/1 will still continue to regulate the current through the load, however abnormal switching of LO and HO may be observed. This poses a problem in terms of switching losses. As previously discussed, the application may need to control the operating frequency to optimize the system efficiency. Excessive high frequency ripple at the DC bus could cause the frequency to become unstable, since this system relies on a self-oscillating principle and is sensitive to noise. Careful attention to the PCB layout is also necessary for this system to operate correctly. If filters on IFB and VCC are not placed correctly, high frequency ripple will couple to the IFB input and interfere with the operation of the control loop. Also if the load current is 1A or 1.5A, when HO turns on the load immediately tries to draw this current. Since the circuit supply is not usually close by, the capacitance of the input wire is not enough to compensate for this large pull of current and this can result in oscillations or change in potential on the input line. To alleviate the circuit of such potential problems it is advisable to implement an input filter. The input filter will also greatly improve the EMC performance.

EMC performance

The IRPLLED1 evaluation board has not been EMC tested. Input and Output filters can be used to reduce the conducted emissions to below the limits of the applicable EMC standard as needed. Inductors may require a powdered Iron core rather than Ferrite, it can handle a much larger current before saturating. If EMC is of critical importance, it may be beneficial to use a MOSFET for the upper switching element and a diode for the lower switch. The reverse recovery time for a diode is inherently shorter than that of a MOSFET and this can help in reducing transients observed in the switching elements resulting in better EMC performance.

Layout Considerations

It is very important when laying out the PCB for the IRS2540/1 based ballast to consider the following points:

1. CVCC2 and CF must be as close to IC1 as possible.
2. The feedback path should be kept to a minimum without crossing any high frequency lines.
3. COUT should be as close to the main inductor as possible.
4. All traces that form the nodes VS and VB should be kept as short as possible.
5. It is essential that all signal and power grounds should be kept separated from each other to prevent noise from entering the control environment. Signal and power grounds should be connected together at one point only, which must be at the COM pin of the IRS2540. The IRS2540 is very sensitive to noise and will not operate if these guidelines are not followed!
   It's a general rule of thumb that all components associated with the IC should be connected to the IC ground with the shortest path possible.
6. All traces carrying the load current need to be adjusted accordingly.
7. Gate drive traces should also be kept to a minimum.

11. Design Procedure Summary

1. Determine the systems requirements: input/output voltage and current needed
2. Calculate current sense resistor
3. Determine the operating frequency required
4. Select L1 and COUT so that they maintain supply into the load during t_HO_on.
5. Select switching components (FET/freewheeling diode) to minimize power losses
6. Determine VCC and VBS supply components
7. Add filtering on the input, IFB and ENN as needed
8. Fine tune components to achieve desired system performance

12. Bill of Materials

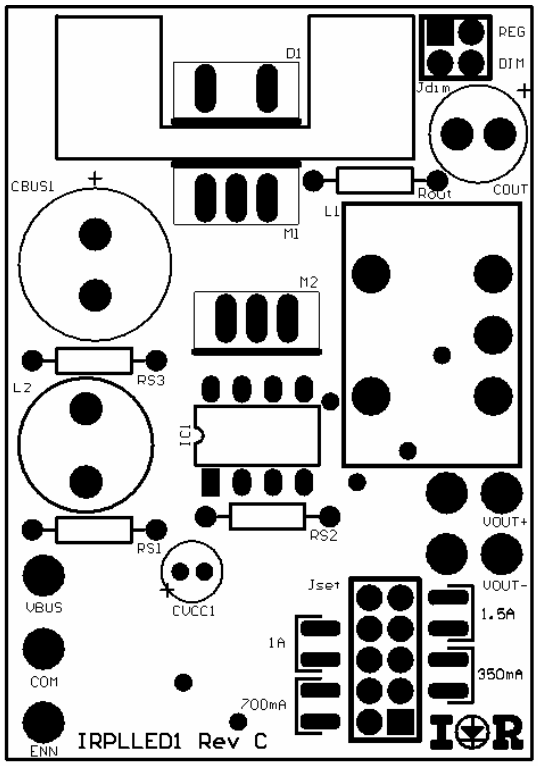
Item	Device Type	Description	Part #	Manufacurer	# of devices	Reference
1	C	10uF, 25V, Radial	UVZ1E100MDD	Nichicon	1	CVCC1
2	C	100nF, 200V, 1812	VJ1812Y104KXCAT	BC Components	1	CBUS2
3	C	100nF, 50V, 0805	VJ0805Y104KXATW1BC	BC Components	3	CVCC2, CBOOT, CEN1
4	C	33uF, 100V	UVZ2A330MPD	Nichicon	1	COUT
5	C	1nF, 50V, 0805	VJ0805Y102KXACW1BC	BC Components	2	CF, CEN2
6	C	47uF, 200V	UVZ2D470MHD	Nichicon	1	CBUS1
7	D	200V, 1A	MUR120T3	On Semi	1	DBOOT
8	D	Mini Melf	LL4148	Diodes Inc	3	DEN1, DVCC, DSYNC
9	D	300V, 8A	8ETH03	IR	1	D1
10	DZ	14V, 0.5W, Mini Melf	ZMM5244B-7	Diodes Inc	1	DCLAMP
11	DZ	7.5V, 0.5W, Mini Melf	ZMM5236B-7	Diodes Inc	1	DOV
12	L	470uH	IL 050 321 31 01	VOGT	1	L1
13	L	470uH	RFB1010-471	Coilcraft	1	L2
14	R	10ohm, 1%, 0805	MCR10EZHF10R0	Rohm	1	RG1
15	R	0.56ohm, 1%, 1206	ERJ-8RQFR56V	Panasonic	3	RCS2, RCS4, RCS6
16	R	0.47ohm, 1%, 1206	ERJ-8RQFR47V	Panasonic	3	RCS1, RCS3, RCS5
17	R	1.43ohm, 1%, 1206	9C12063A1R43FGHFT	Yageo	2	RCS7, RCS8
18	R	100ohm, 1%, 0805	MCR10EZHF1000	Rohm	2	RF, RSYNC
19	R	390ohm, 5%, 1/2W, 2010	ERJ12ZYJ391	Panasonic	1	ROV2
20	R	820ohm, 5%, 1/2W, 2010	ERJ12ZYJ821	Panasonic	1	ROV1
21	R	1k, 5%, 1W	5073NW1K000J12AFX	Phoenix Passive	1	RS2
22	R	47K, 5%, 1W	5073NW47K00J12AFX	Phoenix Passive	1	RS3
23	R	56K, 5%, 1W	5073NW56K00J12AFX	Phoenix Passive	1	RS1
24	R	5ohm, 5%, 1W	5073NW5R100J12AFX	Phoenix Passive	1	Rout
25	IC	IRS2540/1	IRS2540/1	IR	1	In Socket
26	Socket	8 Pin DIP	2-641260-1	Amp	1	IC1
27	M	200V, 16A, TO-220	IRFB17N20D	IR	1	M1
28	T	PC Compact, red	5005	Keystone	2	T1, T4
29	T	PC Compact, black	5006	Keystone	2	T2, T5
30	T	PC Compact, yellow	5009	Keystone	1	T3
31	H	Heatsink	7-340-1PP-BA	IERC	1	
32	B	PCB			1	
33	J	Jumper, 10 Pos.	929836-09-05-ND	3M	1	Jset
34	J	Jumper, 2 Pos.	929836-09-02-ND	3M	1	Jdim
35	SJ	Shorting Jumper	929950-00-ND	3M	3	
36	D	Not Fitted				DIFB
37	R	Not Fitted				RIFB
38	M	Not Fitted				M2
39	TH	TO-220 Insulating Thermal P	SP600-54	Berquist	2	
40	W	Shoulder Washer	3049	Berquist	2	
41	SC	Screw, 4-40, 0.5", Zinc	H346-ND	Building Fasteners	1	
42	N	Nut, 4-40, Hex, Zinc	H216-ND	Building Fasteners	1	

Enable Signal Generator (not included)

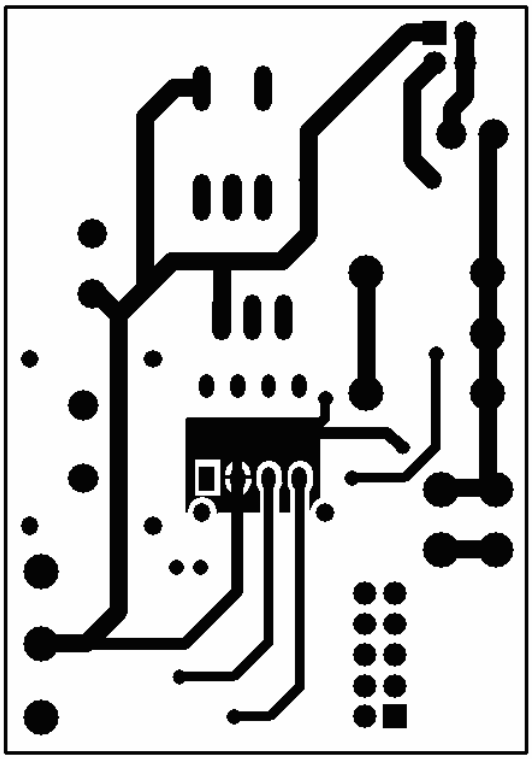
Item	Device Type	Description	Part #	Manufacurer	# of devices	Reference
1	C	10uF, 25V, Radial	ECEA1EKG100	Panasonic	1	CVCC3
2	C	100nF, 50V, 0805	VJ0805Y104KXATW1BC	BC Components	1	CVCC4
3	C	1nF, 50V, 0805	VJ0805Y102KXACW1BC	BC Components	2	C1, C2
4	D	Mini Melf	LL4148	Diodes Inc	1	DEN2
5	R	1k, 1%, 0805	MRC10EZHF1001	Rohm	1	R6
6	R	6.8k, 1%, 0805	MRC10EZHF6801	Rohm	1	R5
7	R	10k, 1%, 0805	MRC10EZHF1002	Rohm	1	R4
8	R	20k	MRC10EZHF2002	Rohm	1	R2
9	R	75k	MRC10EZHF7502	Rohm	2	R1, R3
10	R	Select depending on VBUS		Rohm	1	RS
11	R	56k	MRC10EZHF5602	Rohm	1	R7
12	POT	10k, 10-turn	M64W103KB40	BC Components	1	VR1
13	IC	Comparator	LM393D	Texas Instruments	1	In Socket
14	Socket	8 Pin DIP	2-641260-1	Amp Tyco Electronics	1	IC2
15						

13. PCB Layout

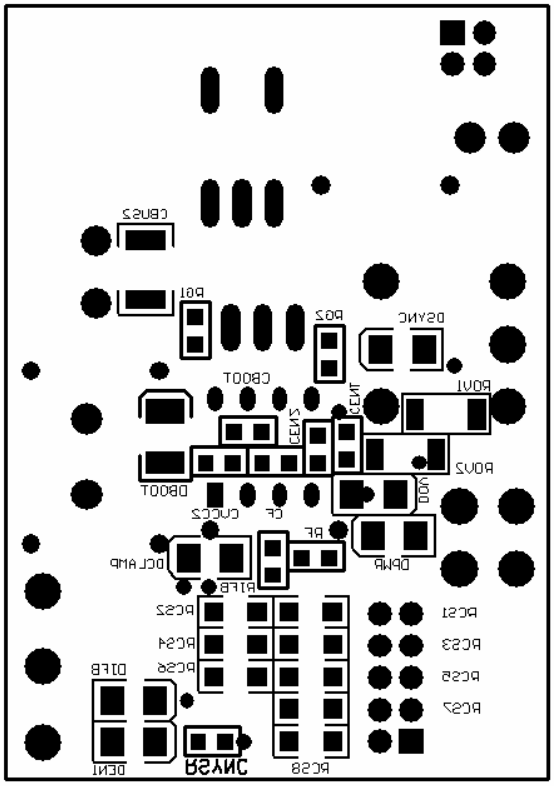
Top Overlay



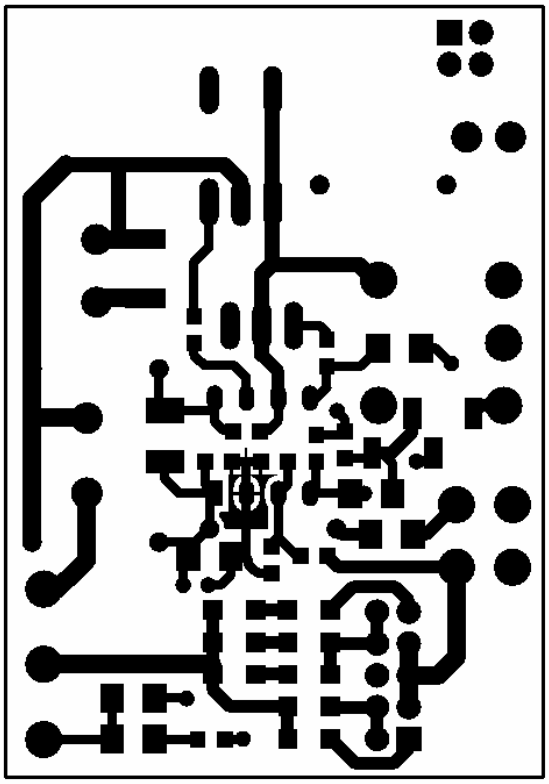
Top Metal



Bottom Overlay



Bottom Metal



Revision History

Rev/Date	Change Description
Rev 2. Aug 1, 2008	**Updated Figure 16 to provide exact schematic of the demo board including sync modification. Added Figure 4a to show LED current jumper settings. Correction made to duty cycle calculation in section 8. Added Figure 28a to show synchronization waveforms for PWM dimming with preceeding explanatory text. New PCB layout added in section 12 to include sync modification.**
Rev 3. Oct 27,2008	**Modified table of contents. Section (1) updated. Section (2) updated. Section (3) updated. Section (4) updated. Section (5) updated. Section (6) updated. Section (8) updated. Section (9) "Open circuit protection" has been re-written with important updates. Later sections have been re-numbered. Updated Fig 22. R7 added to improve PWM dimming signal generator circuit to reduce noise sensitivity and increase stability. R7 also added to signal generator BOM. Section 8 "Dimming Mode" now recommends a PWM frequency of 1kHz for dimming. Added additional comments in "Layout Considerations" item (5)**